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EXAMINER	
LAM, HUNG H	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/089,192	TOYODA ET AL.	
	Examiner	Art Unit	
	Hung H. Lam	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/13/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 12/13/05, have been entered and made of record. Claims 13-20 are added. Claims 1-20 are pending.

In view of the Applicant's amendment of the title, the objection is hereby withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. The drawings are objected to because "pettern recognition" block in Fig. 26 should be changed to "pattern recognition". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after

the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. Figure 13b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1 and 10 are objected to because of the following informalities: in claim 1 line 23 and claim 10 line 8, the "output signal" should be changed to "digital signal". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1-3, 5-8, and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Blessinger (US-5,196,938).

It is noted that the USPTO considers the Applicant's "one of" language to be anticipated by any reference containing one of the subsequent corresponding elements.

With regarding **claim 1**, Blessinger discloses a camera for high-speed image processing, comprising:

photodetector array having plurality photodetectors (Fig. 2; n blocks of an array of photosites), which are arranged two-dimensionally plurality rows and plurality columns (Col. 3, Ln. 30-34) and which are divided into a plurality blocks (Col. 3, Ln. 35-40), the photodetector array repeatedly receiving optical images and generating output signals for the optical images in a plurality of consecutive frames at a predetermined frame rate (Col. 5, Ln. 1-50);

an analog-to-digital converter array (Fig. 1, n ADs) receiving, from the photodetector array, the output signals for the optical images in the plurality of consecutive frames (Col. 3, Ln. 35-44) and generating digital signals in the plurality of consecutive frames (Col. 3, Ln. 45-50), the analog-to-digital converter array including a plurality of analog-to-digital converters in one-on-one correspondence with the plurality of blocks in the photodetector array (Col. 3, Ln. 51-55), each analog-to-digital converter performing analog-to-digital conversion of the output signals which are read sequentially from the photodetectors in the corresponding block (Col. 3, Ln. 65 – Col. 4, Ln. 2: Blessinger teaches multiplexer 22 for selectively outputting a plurality of block

signals to a parallel output 16 which connected to n AD 26. Therefore, it is inherent that each of the A/D in AD 26 can selectively perform analog to digital conversion of a selective block);

an image-processing unit performing predetermined processes on the plurality of consecutive frames of the digital signals (Fig. 1; converter 25; Since the claim language broadly claims to perform a predetermined processes, the Examiner broadly interpreted the parallel to serial convert 25 as an image processing unit for processing parallel data to produce serial data), which are successively transferred from the analog-to-digital converter array and which correspond to the signal outputted from the photodetectors (see Fig. 1), thereby generating processed result signals, other than the output signals for the optical signals (the serial output from converter 25 must be different than raw output signals from the parallel output 16), indicating results of the processes on the plurality of consecutive frames (Col. 3, Ln. 57- Ln. 4, Col. 2).

a selector selecting (Col. 4, Ln 41-43; Blessinger teaches a key pad 38 having suitable switches), among the plurality of consecutive frames, at least one frame based on processed result signals for the plurality of consecutive frames obtained by the image-processing unit (Col. 4, Ln. 41-62).

a signal converter (frame memory 30) converting, into an image signal of a desired frame rate, a least one of the processed result signal (Col. 4, Ln. 1-2; Col. 4, Ln. 15-20; processed result signal is interpreted as the signals that stored in image frame memory 30) and the digital signal from the analog-to-digital converter array to be inputted and thereby outputting an image signal (Col. 4, Ln. 38-40; image signals are played back on monitor 32).

a signal conversion controller (Fig. 1; central controller 36 and memory controller 44) controlling the signal converter to perform the image signal conversion operation for the at least one frame selected by the selector (Col. 4, Ln. 10-20; Col. 4, Ln. 41-66).

With regarding **claim 2,** Gowda in view Blessinger discloses a camera for high-speed image processing wherein the desired frame rate is lower than the predetermined frame rate (Col. 1, Ln. 7-17; Blessinger teaches a camera which records an event at a fast frame rate and plays back the event at a slower frame rate so that the event may be analyzed; therefore, it is inherent that the desired play-back frame rate is slower than the predetermined frame rate/ recording frame rate).

With regarding **claim 3**, Blessinger discloses a camera for high-speed image processing wherein the signal converter (Fig. 1; memory 30) converts either one of the digital signal from the analog-to-digital array and processed result signals into the image signal of the desired frame rate, and outputs the image signal (Col. 4, Ln. 32-40).

With regarding **claim 5,** Blessinger discloses a camera for high-speed image processing wherein the signal converter has a buffer memory (Fig. 1; 30) at a signal input side thereof, the buffer memory storing at least one of the digital signal from the analog-to-digital converter array (Fig. 1; ADC 26) for at least several frames and the processed result signal for at least several frames (Col. 4, Ln. 3-31; Col. 4, Ln. 45-62).

With regarding **claim 6,** Blessinger discloses a camera for high-speed image processing further comprising a data buffer (Fig. 1; source 42) storing predetermined process data (Col. 3, Ln. 65-67; Blessinger teaches a multiplexer 28 inserting the external data source as a header or trailer with the image frame signals from Ads 26; Source 42 must include a data buffer in order to store external data signals), the image-processing unit performing predetermined parallel process, using the predetermined process data, onto digital signals Col. 3, Ln. 67 – Col. 4, Ln. 2) that are transferred from the analog-to-digital converter array and that correspond the signals outputted from photodetectors (see Figs. 1-2; Col. 3, Ln. 25-67).

With regarding **claims 7 and 8,** Blessinger discloses a camera for high-speed image processing wherein the plurality analog-to-digital converters in the analog-to-digital converter array (Fig. 1, n ADs) are provided one-on-one correspondence with the plurality of rows/columns of photodetectors in the photodetector array (Col. 3, Ln. 30-34; Col. 3, Ln. 65 – Col. 4, Ln. 2: Blessinger teaches mux 22 for selectively outputting a plurality of block signals to a parallel output 16 which connected to n AD 26. Therefore, it is inherent that each of the A/D in AD 26 can perform analog to digital conversion of a selective block).

With regarding **claim 10,** Blessinger discloses a camera for high-speed image processing wherein the image-processing unit (Fig. 1; serialize 25) includes least one parallel processing circuit ("one parallel processing circuit" is broadly interpreted as the serialize 25), each of the at least one parallel processing circuit performing a corresponding parallel process on the digital signals (Col. 3, Ln. 65 – Col. 4, Ln. 2; serialize 25 processes parallel data at the input and

provide serial data at the output) that are transferred from the analog-to-digital converter array and that correspond the signals outputted from photodetectors (see circuit diagram in Fig. 1), thereby outputting a processed result signal indicative of the processed result (Col. 3, Ln. 59-64), the selector (Figs. 1-2; Col. 4, Ln. 41-42; Blessinger teaches a key pay 38 having suitable switches) selecting at least one frame based on at least one process result from the at least one parallel processing circuit (Col. 4, Ln. 1-2; Col. 4, Ln. 41-61; Col. 5, Ln. 19: Blessinger teaches key pad 38 with suitable switches control the operation of fast frame recorder; a playback frame must be obtained from the serialized data that are stored in image memory 30), the signal converter (Fig. 1; image memory 30) converting at least one of the digital signal from the analog-to-digital converter array and the processed result signal obtained by the at least one parallel processing circuit (see the circuit diagram in Fig. 1), into the image signal of the desired frame rate, and outputting the image signal (Col. 4, Ln. 33-40; Col. 4, Ln. 1-56; Blessinger teaches a converter for varying the outputted frame rate).

With regarding **claim 11,** Blessinger discloses a camera for high-speed image processing wherein each of the at least one parallel processing circuit (Fig. 1; serialize 25) are provided with several processing elements in one-to-one correspondence with several blocks that make up at least a portion of all the plurality of blocks in the photodetector array (Figs. 1-2 shows that the serialize 25 are provided with 128 parallel signal lines from a corresponding block outputting by the block multiplex 28), each of the several processing elements (128 parallel signal lines) performing a predetermined parallel process on the digital signals (Col. 3, Ln. 59-61) that are transferred from the corresponding analog-to-digital converter (see Fig. 1) and that are

equivalent to the signals outputted from photodetectors existing in the corresponding block (see Fig. 1).

With regarding **claim 12,** Blessinger discloses a camera for high-speed image processing wherein plurality analog-to-digital converters in the analog-to-digital converter array (Fig. 1; Ads 26) are provided one-to-one correspondence with the plurality rows photodetectors the photodetector array (Col. 3, Ln. 30-40; Col. 3, Ln. 65 – Col. 4, Ln. 2: Blessinger teaches mux 22 for selectively outputting a plurality of block signals to a parallel output 16 which connected to n AD 26. Therefore, it is inherent that each of the A/D in ADs 26 can selectively perform analog to digital conversion of a selective block), each of the at least one parallel processing circuits (serialize 25) including several processing elements (128 parallel signal lines) which are provided in one-to-one correspondence with several rows that make up least portion all the plurality of rows the photodetector array (Col. 3, Ln. 30-40), each of the several processing elements performing predetermined parallel process on digital signals (Col. 3, Ln. 59-61) that are transferred from analog-to-digital converter array that equivalent to the signals outputted from the photodetectors in the corresponding row (see Fig. 1).

With regarding **claim 13,** Blessinger discloses a camera for high-speed image processing, wherein the selector (Col. 4, Ln. 41-43) selects at least one frame that includes one frame, processed results (Col. 4, Ln. 44-61; Blessinger teaches the keypad 38 with suitable switches to control the operation of the fast frame recorder 10) thereof obtained by the image-processing

unit satisfying a predetermined condition (Col. 5, Ln. 1-57; a frame rate of 1000 frame per second requires an exposure time of 1/1000 second).

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claim 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blessinger in view of Onishi (US-6,636,254).

With regarding **claim 4,** Blessinger teaches a camera for high-speed image processing wherein the signal converter (Fig. 1; image memory 30) converts signals into image signal of the desired frame rate (Col. 4, Ln. 32-40), and outputs the image signal (Fig. 1; Col.4, Ln. 55-61).

However, Blessinger fails to explicitly disclose a camera for high-speed image processing wherein the signal converter combines the digital signal from the analog-to-digital converter array and the processed result signal and outputs the image.

In the same field of endeavor, Onishi teaches an image converter having an image synthesizer circuit (Fig. 10; image synthesizer 22) for synthesizing raw image data from a first and second optical signals (Col. 12, Ln. 61-67 – Col. 13, Ln. 1-3) with inverting image data of the first and second optical signals (Fig. 10; image inverting circuit 11a-b provide inverting image data of the first and second optical signals). Onishi further teaches that the synthesizing result produces a desired picture-in-picture image and selectively outputs to a monitor (Fig. 10;

21 ; Col. 13, Ln. 4-13). In light of the teaching from Onishi, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Blessinger by having an image converter claimed by Onishi in order to display different images among transformed images. The modifications thus allow the monitor to display desired picture-in-picture images (Onishi: Fig. 10; 21 ; Col. 13, Ln. 4-13).

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blessinger in view of Gowda (US-6,115,066).

With regarding **claim 9,** Blessinger teaches a camera wherein an image-processing unit (mux 25) performs a parallel to serial conversion from a plurality of parallel data output of the analog-to-digital converter array (Fig. 1; Ads 26; Col. 3, Ln. 65 – Col. 4, Ln.2).

However, Blessinger fails to disclose a camera for high-speed image processing wherein the image-processing unit includes a plurality processors one-to-one correspondence with the plurality of photodetectors, the plurality of processors performing parallel processes on the digital signals that are transferred from the analog-to-digital converter array and that correspond to the signals outputted from the plurality of photodetectors.

In the same field of endeavor, Gowda teaches a camera wherein a plurality of analog-to-digital converter (40_1-40_N) connects to a plurality of column of pixels 30 (Fig. 3; AD 40_1-40_N and column of pixels 30). Gowda further teaches that each of the output of the analog-to-digital converter (40_1-40_N) connect to one of a correlated double sampling circuitry in order to perform noise reduction in each columns and minimize the on-chip circuitry (Fig. 3; A/D converter 40_1-

40_N, and array of pixels 30; Col. 3, Ln. 29-38; Col. 4, Ln. 50 –Col. 5, Ln. 15). In light of the teaching from Gowda, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Blessinger by including a double correlated sampling circuitry in each output of the A/D as claimed by Gowda in order to perform parallel noise reduction process in a plurality of columns of an image sensor. The modifications thus provide better image quality and minimize the on-chip circuitry (Gowda: Col. 3, Ln. 29-38).

11. Claims 14, 15, 17, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blessinger in view of Koezuka (US-4,805,224).

With regarding **claim 14,** Blessinger fails to explicitly disclose a camera for high-speed image processing, wherein the selector judges whether or not the processes results for the consecutive frames satisfy the predetermined condition, determines one frame, processed results thereof satisfying the predetermined condition, and selects at least one frame including the determined one frame.

In the same field of endeavor, Koezuka teaches a camera system wherein a pattern matching circuit perform comparison of a master pattern in a master pattern memory 7 and an image of an object pattern in a frame memory 6 (Col. 2, Ln. 65-68). Koezuka further teaches the object with the highest degree of matching to the master pattern is selected by the pattern matching circuit 9 for sending to control circuit 10 as a desired pad position (Fig. 1; pattern matching circuit 9; Col. 3, Ln. 1-5; pattern matching circuit 9 must include a selector for selecting an object with the highest degree of matching to the master pattern). In light of the

teaching from Koezuka, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Blessinger to select an object with the highest degree of matching to the master pattern as claimed by Koezuka in order to signal a desired position to control circuit 10. The modifications thus provide highly pattern recognition rate and accurate positioning (Koezuka: Col. 1, Ln. 44-46).

With regarding **claim 15,** Blessinger fails to disclose a camera for high-speed image processing, wherein the image processing unit performs a characteristic extracting process on the plurality of consecutive frames of the digital signals to determine characteristics of the consecutive frames, and wherein the selector judges whether or not the extracted characteristics of the consecutive frames satisfy the predetermined condition, determines one frame, a characteristic thereof satisfying the predetermined condition, and selects at least one frame including the determined one frame.

In the same field of endeavor, Koezuka teaches a camera system wherein a pattern matching circuit perform comparison of a master pattern in a master pattern memory 7 and an image of an object pattern in a frame memory 6 (Col. 2, Ln. 65-68). Koezuka further teaches the object with the highest degree of matching to the master pattern is selected by the pattern matching circuit 9 for sending to control circuit 10 as a desired pad position (Fig. 1; pattern matching circuit 9; Col. 3, Ln. 1-5; pattern matching circuit 9 must include a selector for selecting an object with the highest degree of matching to the master pattern). In addition, Koezuka teaches an extraction circuit (81) operating to store the next extract pattern (Fig. 2; extraction circuit 81; Col. 3, Ln. 22-68; the object with the highest degree of matching to the

master pattern is selected by the pattern matching circuit 9; the matching circuit 9 must also judge whether or not the extracted object satisfy the highest degree of matching to the master pattern). In light of the teaching from Koezuka, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Blessinger to select an object with the highest degree of matching to the master pattern as claimed by Koezuka in order to signal a desired position to control circuit 10. The modifications thus provide highly pattern recognition rate and accurate positioning (Koezuka: Col. 1, Ln. 44-46).

With regarding **claim 17,** Blessinger discloses a camera for high-speed image processing, wherein the image processing unit performs a pattern matching process on the plurality of consecutive frames of the digital signals to generate the processed result signals indicating whether or not a predetermined pattern is detected in the consecutive frames (Col. 2, Ln. 64-Col. 3, Ln. 21), and wherein the selector determines (Fig. 1; pattern matching circuit 9), based on the process result signals, one frame in which the predetermined pattern is detected (Col. 3, Ln. 22-46), and selects at least one frame including the determined one frame (Col. 3, Ln. 1-5).

With regarding **claim 18,** Blessinger discloses a camera for high-speed mage processing, wherein the image-processing unit includes a parallel processing circuit (Fig. 1; serialize 25) that performs a parallel process on the plurality of consecutive frames of the digital signals to generate the processed result signals (Col. 3, Ln. 59-61).

However, Blessinger fails to explicitly disclose that the processed result signals indicative of whether or not the consecutive frames of the digital signals satisfy a predetermined condition,

and wherein the selector selects at least one frame that includes one frame, a processed result signal thereof indicating that the subject frame satisfies the predetermined condition.

In the same field of endeavor, Koezuka teaches a camera system with a pattern matching circuit wherein the object with the highest degree of matching to the master pattern is selected by the pattern matching circuit 9 for sending to control circuit 10 as a desired pad position (Fig. 1; pattern matching circuit 9; Col. 3, Ln. 1-5; pattern matching circuit 9 must include a selector for selecting an object with the highest degree of matching to the master pattern). Koezuka further teaches an extraction circuit (81) operating to store the next extract pattern (Fig. 2; extraction circuit 81; Col. 3, Ln. 22-68; the extracted object must also indicates whether it satisfies the highest degree of matching since it is compared with the master pattern in memory 7). In light of the teaching from Koezuka, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Blessinger to select an object with the highest degree of matching to the master pattern as claimed by Koezuka in order to signal a desired position to control circuit 10. The modifications thus provide highly pattern recognition rate and accurate positioning (Koezuka: Col. 1, Ln. 44-46).

With regarding **claim 20,** the claim contains the same limitations as claimed in claim 17. Therefore, claim 20 is analyzed and rejected as discussed in claim 17.

Allowable Subject Matter

12. Claims 16 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 16 the following is a statement of reason for the indication of allowance: the prior art made of record and considered pertinent to the applicant's disclosure does not disclose nor fairly suggest a camera for high-speed image processing of claim 15 further in combination with: **wherein the image processing unit performs a center of gravity calculation process on the plurality of consecutive frames of the digital signals to determine the locations of the centers of gravity in the consecutive frames of the digital signals, and wherein the selector judges whether or not the locations of centers of gravity in the consecutive frames satisfy the predetermined condition, determines one frame, locations of the center of gravity thereof satisfying the predetermined condition, and selects at least one frame including the determined one frame.**

Regarding claim 19 the following is a statement of reason for the indication of allowance: the prior art made of record and considered pertinent to the applicant's disclosure does not disclose nor fairly suggest a camera for high-speed image processing of claim 18 further in combination with: **wherein the parallel processing circuit performs a center of gravity calculation process on the plurality of consecutive frames of the digital signals to generate the processed result signals indicative of the locations of the centers of gravity in the consecutive frames of the digital signals, and wherein the selector judges, based on the**

processed result signals, whether or not the locations of centers of gravity of the consecutive frames satisfy the predetermined condition, determines one frame, locations of the center of gravity thereof satisfying the predetermined condition, and selects at least one frame including the determined one frame

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung H. Lam whose telephone number is 571-272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NGOC YEN VU can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HL
04/03/06

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER